GMAC IP Brief

Overview

SoCtronics is a customer-focused VLSI design and embedded software service company operating since 2003. The company has operating entities in Hyderabad, India and Santa Clara, California. SoCtronics offers complete spec-to-silicon turnkey solutions that include embedded systems and software/firmware co-development. The company has over 500 employees world-wide and is privately owned and operated.

India's Soctronics claims 28-nm design win
Peter Clarke
10/19/2011 8:19 AM EDT
EE Times

GMAC Description

GMAC IP is responsible for transmitting and receiving Ethernet frames as per IEEE 802.3 standard. It supports various PHYs like MII/GMII/RGMII at various speeds like 10/100/1000Mbps. It also supports half-duplex mode in MII mode. It also has various offload features like IPv4/TCP/UDP checksums for both transmit and received packets. GMAC IP can also generate CRC for all transmitted packets. It fetches data from the host memory to be transmitted on to the PHY and also writes the received packets into the host memory for further processing. GMAC IP supports usage of 4 queues for efficient processing of the received packets, based on Receive Side Scaling (RSS) proposed by Microsoft. GMAC IP supports usage of legacy interrupts (INTx) as well as MSI-x interrupts to make use of multiple receive queues. On transmit side, GMAC IP supports 1 queue. It has and MDIO interface to communicate with the PHY for constant probing of the link status.

Configurable Features:

The IP provides various configurable options

- AXI 32-bit or 64-bit system interface for data path
- Configurable AXI write FIFO depth
- Configurable checksum offloads
- Configurable stripping of VLAN tags and CRC on receive packets
- Configurable default queue to direct all packets to the same queue
- Configurable PHY interface to support MII/GMII and RGMII interfaces
- Configurable transmit offloads like insertion or replacement of VLAN tags, replacement of source addresses, insertion of IPv4/TCP/UDP checksums
- Configurable option to enable padding of data and CRC appending for all outgoing packets
- Configurable receive offloads to strip VLAN and CRC, IPv4/TCP/UDP checksum offloads
- Configurable RSS key to manipulate the RSS queues on receive side

GMAC IP Features:

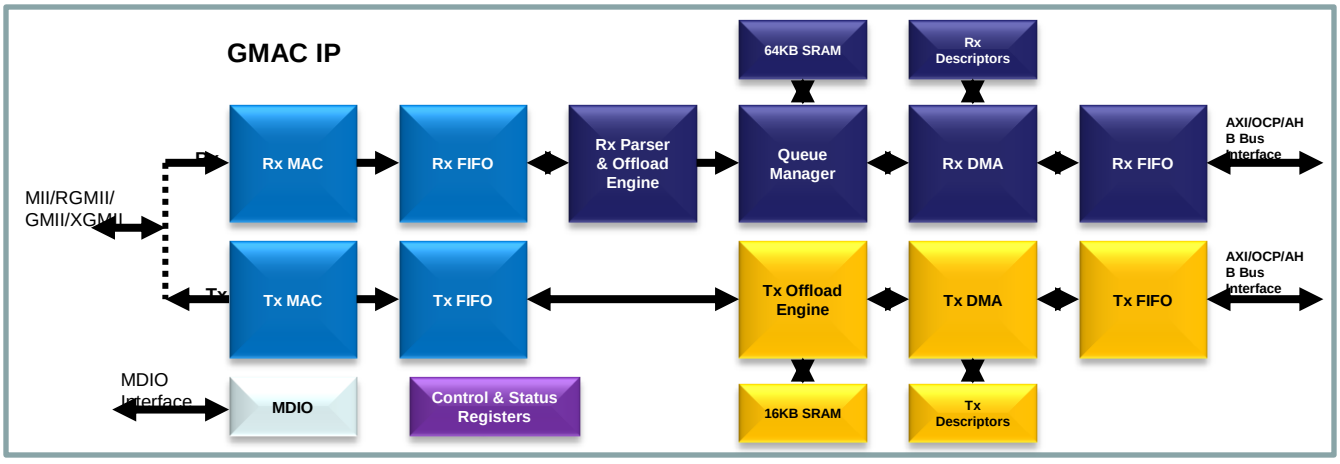
- Compliant with IEEE 802.3 standard
- Supports AMBA 2.0 for AHB slave ports
- Supports AMBA 3.0 for AXI master ports
- Configurable to support data transfer rates of 10/100/1000Mbps
- Supports both full duplex and half duplex operation
- Supports CSMA/CD protocol for half duplex
- Automatic CRC and pad generation controllable on a per frame basis (Transmit side)
- Programmable inter frame gap
- Source address field insertion or replacement, VLAN insertion or replacement on a per frame basis
- IPv4/TCP/UDP checksum offloads enabled per frame basis while transmitting packets
- Preamble and start-of-frame delimiter insertion in transmit and deletion in receive paths
- VLAN based filtering based on hash
- Multicast filtering based on hash
- Configurable to pass all unicast, multicast frames by enabling of promiscuous mode
- CRC and VLAN tag stripping on received frames
- Support for MII/GMII/RGMII PHY interfaces
- Pause frame generation based on receive buffer full (configurable threshold) level
- Option to forward packets with CRC error or receive error
- Option to forward packets with length error
- Configurable packet sizes beyond which transmission should start without waiting for entire packet
- Configurable IPv4/TCP/UDP checksum offloads on receive side
- 4 receive queues based on RSS defined by Microsoft
- Optimal queue based dynamic memory management to manage receive queues with 64KB buffer
- 8 interrupt sources generating 6 interrupts
- INTx and MSI-x supported for interrupts
- Large Segment Offload (LSO) on Transmit path
- Capable of sending pause frames when internal buffers are full
- Pre-fetch of 64 receive buffers for better bandwidth in receive path
- Supports 64-bit AXI address width
- Low power features to support wakeup with wake-on-LAN packets, unicast packets or with link state change event
- Supports internal loopback on the GMII/MII for debugging
- MDIO support to read/write to the PHY level registers
- Provides debug port interface for GMAC core debug
- Statistics counters to give information on IP data like packets transmitted/received or packets dropped etc
- Support to stop operations of all existing transactions at logical boundary (AXI, AHB and MAC interfaces)
- Internal clock and reset blocks to generate the corresponding clocks and resets to all the blocks of the IP

SoCtronics Quick Facts

- Started operations in 2003
- Privately owned and operated
- Design centers and sales offices in Santa Clara, California and Hyderabad, India
- 500+ employees world wide

Engagement Models

- Point task and augmentation
- Turnkey with Spec to SOW to Deliverables
- Off-shore Design Center with Experts On Demand benefits
  - Staff and facilities in India
  - Operated by SoCtronics
  - Directed by client



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